DENSE-PAC
MICROSYSTEMS

M-Densus
High Density Memory Device

128 Megabit Synchronous DRAM
### DPSD16MX8RKY5

PRELIMINARY

DESCRIPTION:

The *M-Densus* series is a family of interchangeable memory modules. The 128 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 8 Meg x 8 SDRAMs.

This 64 Megabit based *M-Densus* module, the DPSD16MX8RKY5 has been designed to fit in the same footprint as the 8 Meg x 8 SDRAM TSOP monolithic and 64 Megabit SDRAM based family of *M-Densus* modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:

- Configuration Available:
    16 Meg x 8 (2 Banks of 2M x 4 x 8 bits)
- Clock Frequency:
    $66^{[1]}$, $83^{[1]}$, 100, $125^{[2]}$, $133^{[2]}$ MHz (max.)
- PC100 and PC133 Compatable
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack
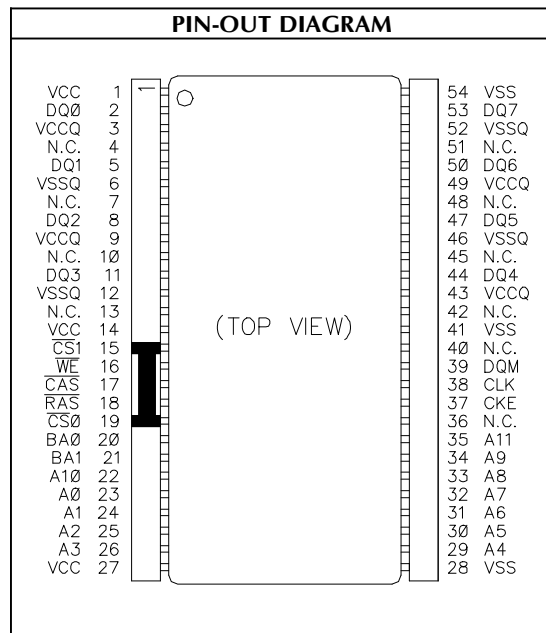
NOTES: [1] Available in Military and Industrial Temperature Ranges Only.
          [2] Available in Commercial Temperature Range Only.

PIN-OUT DIAGRAM

VCC	1		54	VSS
DQØ	2		53	DQ7
VCCQ	3		52	VSSQ
N.C.	4		51	N.C.
DQ1	5		5Ø	DQ6
VSSQ	6		49	VCCQ
N.C.	7		48	N.C.
DQ2	8		47	DQ5
VCCQ	9		46	VSSQ
N.C.	1Ø		45	N.C.
DQ3	11		44	DQ4
VSSQ	12		43	VCCQ
N.C.	13	(TOP VIEW)	42	N.C.
VCC	14		41	VSS
$\overline{CS1}$	15		4Ø	N.C.
$\overline{WE}$	16		39	DQM
$\overline{CAS}$	17		38	CLK
$\overline{RAS}$	18		37	CKE
$\overline{CSØ}$	19		36	N.C.
BAØ	2Ø		35	A11
BA1	21		34	A9
A1Ø	22		33	A8
AØ	23		32	A7
A1	24		31	A6
A2	25		3Ø	A5
A3	26		29	A4
VCC	27		28	VSS

PIN NAMES

A0 - A11	Row Address: A0 - A11 Column Address: A0 - A8
BA0, BA1	Bank Select Address
DQ0 - DQ7	Data In / Data Out
$\overline{CAS}$	Column Address Strobes
$\overline{RAS}$	Row Address Enables
$\overline{WE}$	Data Write Enable
DQM	Data Input/Output Mask
CKE	Clock Enable
CLK	System Clock
$\overline{CS}0$-$\overline{CS}1$	Chip Selects
V_{CC}/V_{SS}	Power Supply/Ground
V_{CCQ}/V_{SSQ}	Data Output Power/Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM
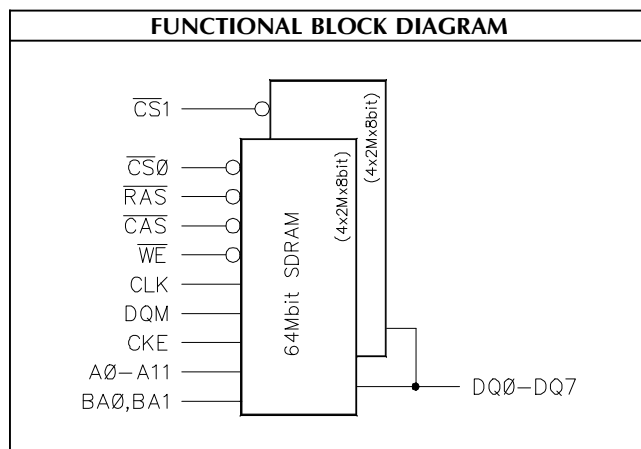
PRELIMINARY

PART NUMBER DESCRIPTION

DP SD 16M X 8 RK Y5 – DP – XX   XX   X   X

PREFIX TYPE MEMORY DESIG MEMORY DESIG PACKAGE SUPPLIER MEMORY SPEED CL GRADE
               DEPTH   WIDTH

Blank	Commercial Temperature
I	Industrial Temperature
M	Military Temperature
2	CAS LATENCY 2
15 [1]	15ns (66MHz)[1]
12 [1]	12ns (83MHz)[1]
10	10ns (100MHz)
08 [2]	8ns (125MHz)[2]
75 [2]	7.5ns (133MHz)[2]
P1	PC100

MANUFACTURER CODE[3]

SUPPLIER CODE[3]

STACKABLE TSOP

64 MEGABIT (8Mx8) LVTTL BASED

MEMORY MODULE WITHOUT SUPPORT LOGIC

SYNCHRONOUS DRAM

NOTES: [1] Available in Military and Industrial Temperature Ranges Only.
         [2] Available in Commercial Temperature Range Only.
         [3] Contact your sales representative for supplier and manufacturer codes.

MECHANICAL DRAWING

PIN 1
INDEX

TOP VIEW   SIDE VIEW   BOTTOM VIEW

.885±.006

.020

.0315

.0305

0.098 MAX.   .0335

Standard TSOP Pad Layout is acceptable, however, when possible, the following Pad Layout is recommended for optimal manufacture and inspection. See Application Note 53A001-00 for further information.

END VIEW

.502±.006

0.0315 BSC

0.022
0.018

0.407   0.527
0.397   0.517

0.819 BSC
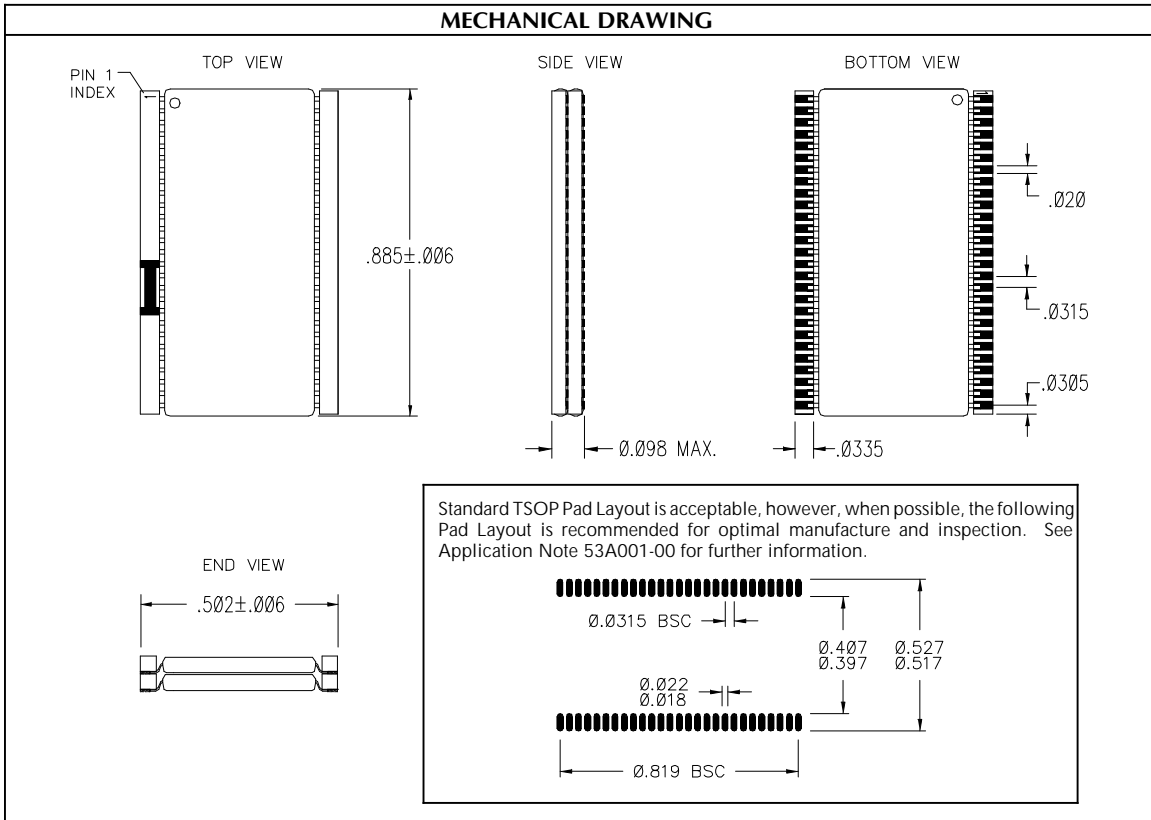
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